13.1 A CMOS Temperature Sensor with a 3σ Inaccuracy of ±0.1°C from –55°C to 125°C

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This paper presents the first CMOS smart temperature sensor that is accurate to within ±0.1°C over the full military temperature range of –55°C to 125°C. This level of accuracy represents a 5-fold improvement in the state of the art [1,2]. This improvement is achieved by reducing circuit errors to the 0.01°C level through the extensive use of offset cancellation and dynamic element matching, combined with a room-temperature calibration.

The operating principle of the sensor is illustrated in Fig. 13.1.1. Two substrate PNP transistors Q_1 and Q_2 are biased at a 5:1 current ratio. The difference in their base-emitter voltages ΔV_{BE} is then proportional to absolute temperature (PTAT), and is digitized by a ΔΣ modulator. When the modulator's bitstream output bs=0, its input is $16{\cdot}\Delta V_{BE}$, and when bs=1, its input is $-V_{BE}$, the base-emitter voltage of a third transistor Q_3. Since the modulator's feedback ensures that the average input is zero, the average value of the bitstream $\mu = 16{\cdot}\Delta V_{BE} / (V_{BE} + 16{\cdot}\Delta V_{BE})$. This is the ratio of a PTAT voltage and a bandgap voltage, and is thus a digital representation of the chip's temperature [1]. The accuracy of this ratio is limited by V_{BE}, which varies with the saturation current of Q_3 and the absolute value of the bias current I_{trim} [3]. At a single temperature, I_{trim} is adjusted to correct for the resulting temperature errors. This is done after packaging to incorporate the effects of mechanical stress.

The front-end circuit that generates ΔV_{BE} and V_{BE} is shown in the right half of Fig. 13.1.2. A single pair of transistors Q_L and Q_R is used to generate both voltages. When bs=0, a multiplexer selects ΔV_{BE} as the modulator's input voltage $V_{\Delta\Sigma}$. A set of 6 current sources, each with a nominal value of 1μA, is used to make a dynamically matched 5:1 bias current ratio [3]. The current source that generates the unit current is interchanged whenever bs=0, which ensures that any mismatches average out [4]. To average out mismatch between Q_L and Q_R, their bias currents are swapped within a ΔΣ cycle (using the control signal ϕ_L). The modulator then effectively processes the average of the two ΔV_{BE}s.

When bs=1, the multiplexer first selects V_{BEL} (ϕ_L=1) and then V_{BER} (ϕ_L=0). The average of the two is processed by the modulator. The bias current for the selected transistor is generated using the same six current sources mentioned above. One of them is switched on and off during consecutive ΔΣ cycles using the bitstream *trim_bs* of an 8b digital first-order ΔΣ modulator [5], while the other 5 are either on or off. This results in a bias current I_{trim} that can be programmed between 0μA and 6μA with a resolution of 4nA, or 0.01°C. The quantization noise in *trim_bs* is averaged out by the analog ΔΣ modulator, while intermodulation between *trim_bs* and *bs* (a problem unsolved in [5]) is prevented by freezing the digital modulator when bs=0.

The bias currents are generated by a chopped bias circuit (left half of Fig. 13.1.2) in such a way that V_{BE} is not affected by the spread of the current gain β of the PNPs. Two transistors Q_{BL} and Q_{BR}, biased at a 1:10 current ratio, have a difference in base-emitter voltage $\Delta V_{BE,bias}$. They are incorporated in a feedback loop with an opamp and resistors R_{1a} (with the switches in the position shown) and $R_2 = R_{1a} / 10$. The feedback ensures that $I = 2(\beta+1)/\beta \cdot \Delta V_{BE,bias}/R_{1a}$. When applied to the emitter of Q_L or Q_R, this results in a *collector* current proportional to $\Delta V_{BE,bias}/R_{1a}$, making the generated V_{BE} independent of β. Opamp offset and PNP mismatch are eliminated by chopping the bias circuit with the control signal ϕ_L. The generated V_{BE} is also insensitive to the supply voltage because all current sources are cascoded (not shown) and have matched output voltages.

The second-order ΔΣ modulator and its timing diagram are shown in Fig. 13.1.3 and Fig. 13.1.4. The first integrator uses correlated double-sampling (CDS) to reduce offset and 1/*f* noise [2] and is built around a gain-boosted opamp. In phase ϕ_1, the opamp has unity gain and the input voltage $V_{\Delta\Sigma}(\phi_1)$ is sampled on one or more of the sampling capacitors C_S (8pF each). In phase ϕ_2, the integration capacitors C_{int} (20pF) are switched into the feedback loop of the opamp while the input changes to $V_{\Delta\Sigma}(\phi_2)$. As a result, a charge of $k{\cdot}C_S{\cdot}[V_{\Delta\Sigma}(\phi_1)–V_{\Delta\Sigma}(\phi_2)]$ is integrated, where k is the number of sampling capacitors selected. When integrating V_{BE} (bs=1), only one sampling capacitor is used (k=1), while all eight capacitors are used for ΔV_{BE} (k=8). An additional factor of two is obtained by integrating ΔV_{BE} *twice* per ΔΣ cycle, resulting in the desired total gain of 16. Capacitor mismatch is averaged out by interchanging the capacitor used to sample V_{BE} during consecutive ΔΣ cycles [4]. The output of the first integrator plus a scaled version of $V_{\Delta\Sigma}$ are input to the second integrator. At the end of every ΔΣ cycle, a comparator evaluates the polarity of the output of that integrator and determines the value of *bs* for the next cycle.

To ensure that the modulator's offset contributes less than 0.1°C to the temperature error, the complete modulator is chopped as the residual offset after CDS is still too large. To avoid disturbing the operation of the modulator when chopping, its state is also inverted by swapping the integration capacitors of both integrators (Fig. 13.1.3). Since the modulator is chopped only twice per conversion (Fig. 13.1.4), the charge injection of the chopper switches has a negligible effect.

The modulator runs at a clock frequency of 16kHz, which gives a resolution of 0.01°C at 10 conversions per second. The bitstream is decimated using an off-chip sinc^2 filter, which has been made slightly non-linear to correct for systematic non-linearity.

The temperature sensor is fabricated in a standard low-cost 0.7μm CMOS process with linear capacitors (Fig. 13.1.7). Figure 13.1.5 shows a performance summary. Figure 13.1.6 shows the measured temperature error for 24 devices mounted in ceramic DIL packages and calibrated at 30°C using a platinum resistor thermometer with an inaccuracy of ±0.02°C. Over the range of –55°C to 125°C, the 3σ inaccuracy of the devices is less than ±0.1°C. This is more than 5× better than the best results published to date [1].

Acknowledgement
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References
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[2] C. Hagleitner et al., "A Gas Detection System on a Single CMOS Chip Comprising Capacitive, Calorimetric, and Mass-Sensitive Microsensors," *ISSCC Dig. Tech. Papers,* pp. 430-431, Feb., 2002.
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[4] M.A.P. Pertijs, J.H. Huijsing, "A Sigma-Delta Modulator with Bitstream-Controlled Dynamic Element Matching," *Proc. ESSCIRC,* pp. 187-190, Sept., 2004.
[5] G. van der Horn, J.H. Huijsing, "Smart Temperature Sensor with Integrated Bitstream Calibration," *Proc. ESSCIRC*, pp. 234-237, Sept., 1995.

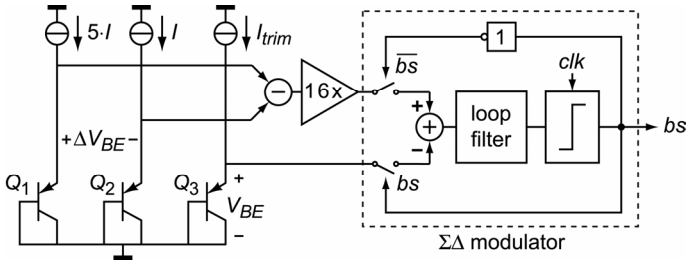

Figure 13.1.1: Operating principle of the temperature sensor.

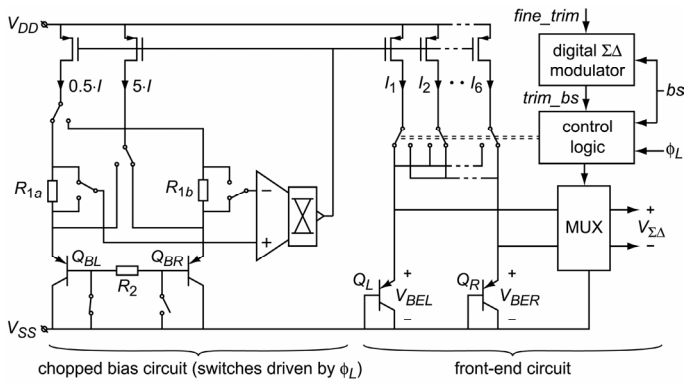

Figure 13.1.2: Circuit diagram of the bias and front-end circuits.

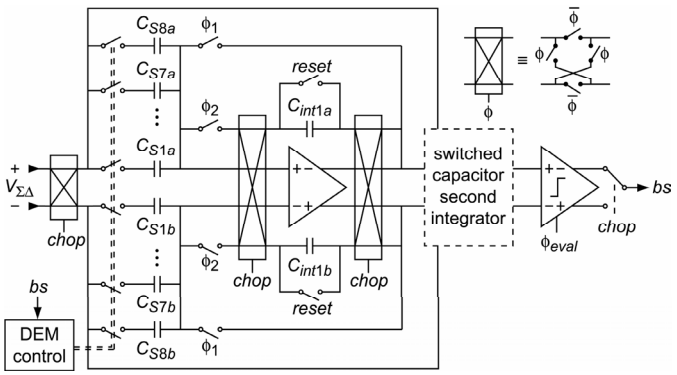

Figure 13.1.3: Circuit diagram of the ΔΣ modulator.

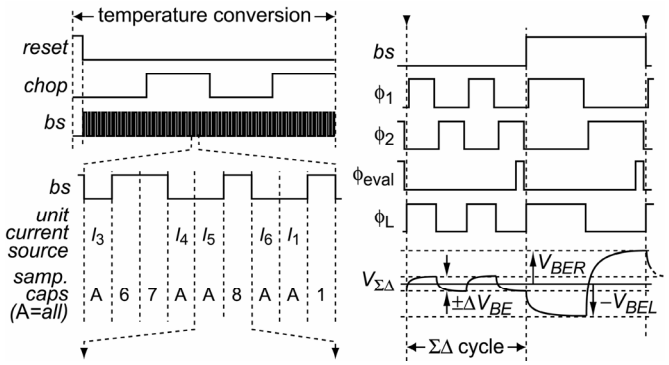

Figure 13.1.4: Timing diagram of a temperature conversion, showing details of a fragment of the bitstream and the timing within a ΔΣ cycle.

Technology	0.7μm 2M-1P analog CMOS	
Chip size	4.5mm²	
Supply voltage	2.5V – 5.5V	
Temperature range	-55°C – 125°C	
Resolution (rms noise level)	0.01°C 0.002°C	10 conversions/s 1 conversion/s
Supply current	75μA	continuous operation
Power supply sensitivity	0.03°C/V	2.5V–5.5V

Inaccuracy (3σ)	±0.03°C	30°C
	±0.1°C	-55°C – 125°C

Figure 13.1.5: Performance summary.

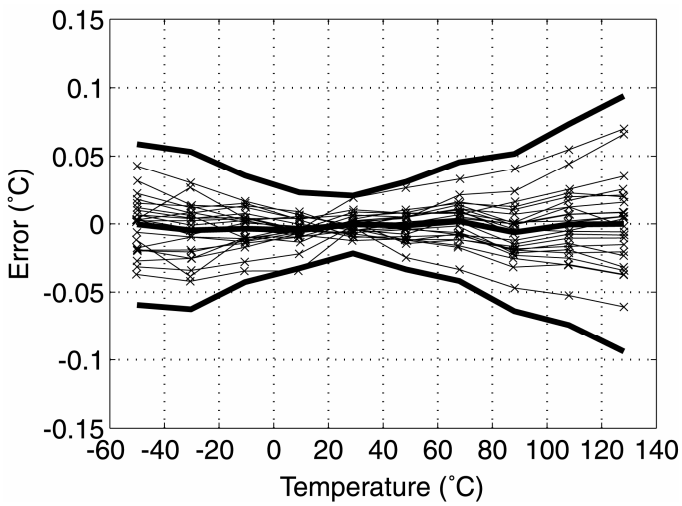

Figure 13.1.6: Measured temperature error of 24 devices with average and ±3σ values.

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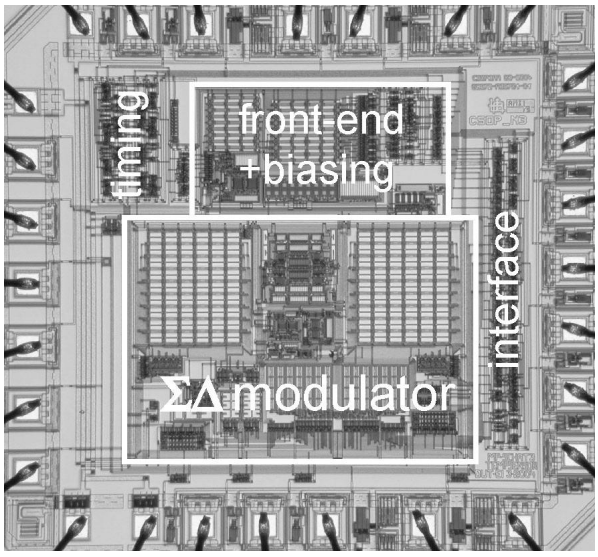

Figure 13.1.7: Chip micrograph of the temperature sensor.

